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Voltage Sag Compensation Scheme for DVR using Space Vector Modulation

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Abstract: This paper deals with improving the voltage quality of loads from voltage sags using dynamic voltage restorer (DVR). The higher active requirement associated with pulse width modulation (PWM) has caused a substantial rise in size and cost. The existing control strategies either mitigate the pulse width modulation or improve the utilization of dc link energy reducing the amplitude of injected voltage. In this paper on enhanced sag compensation strategy is proposed it mitigate the overall sag compensation time. An analytical study shows that the proposed method significantly increases the DVR support time compared with existing PWM method. This enhancement can also be seen as a considerable reduction in dc link capacitor sixe for new installation. The performance of the proposed method is evaluated using simulation study and finally verified experimentally on a small prototype model.

Keywords: Dynamic voltage restorer (DVR), voltage phase jump compensation, voltage sag compensation, Pulse Width Modulation.

I. INTRODUCTION

IN industrial distribution systems, the grid voltage disturbances (voltage sags, swells, flicker, and harmonics) are the most common power quality problems [1]. Sag, being the most frequent voltage disturbance, is typically caused by a fault at the remote bus and is always accompanied by a phase angle jump. The phase jump in the voltage can initiate transient current in the capacitors, transformers, and motors [2]. It can also disturb the operation of commutated converters and may lead to glitch in the performance of thyristor-based loads [3]. It is therefore imperative to protect sensitive loads, especially from the voltage sags with phase jump [4].

To protect sensitive loads from grid voltage sags, custom power devices (such as SVC, D-STATCOM, dynamic voltage restorer (DVR), and UPQC) are being widely used [5]-[8]. Among these devices, DVR has emerged as the most cost-effective and comprehensive solution [9]-[11]. The system configuration of a DVR is shown in Fig. 1. It consists of a dc link capacitor (serving as an energy reserve for DVR), a is to inject a voltage with certain magnitude and phase in series with the upstream source voltage such that the load connected downstream always sees the pure sinusoidal voltage at its terminals.

Numerous control strategies for DVR have been reported in the literature [12]. The emphasis is on either reducing the voltage rating of DVR by aligning the injected voltage with the source voltage (i.e., in-phase compensation) or minimizing the dc storage capacity by using the reactive power compensation/energy-optimized approach [12]-[14]. All of these methods, however, cannot correct the phase jump and thus can result in premature tripping of sensitive loads [15].

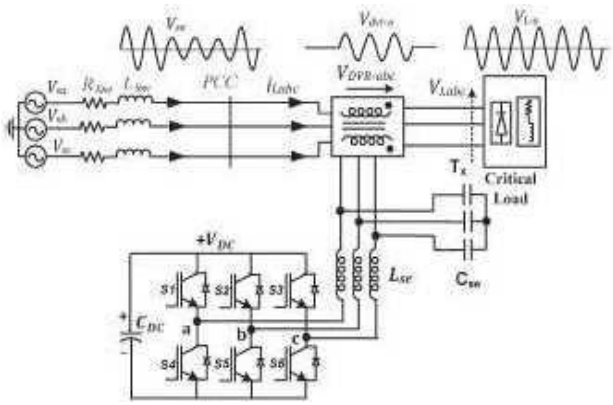

Fig. 1. Basic DVR-based system configuration

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The only possible way to mitigate the phase jump is to restore the load voltage to the pre fault value. Such an approach is addressed as presag compensation in [13]. However, the phase jump compensation using the presag method requires a significant amount of active power from the dc link capacitor. Thus, this method will require a larger size capacitor or will resultin shorter sag support time. In [16] and [17], an interesting technique is proposed

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to increase the compensation time while mitigating the voltage phase jump. In this method, once the dc link voltage drops to the threshold limit, the magnitude of the injected voltage is reduced by synchronizing the phase-locked loop (PLL) to the grid voltage. This allows further utilization of the dc link capacitor energy and extends the compensation time by some extent. However, it continues to consume the energy in the dc link capacitor throughout the duration of compensation and imposes limitation on compensation time enhancement topologies for DVR

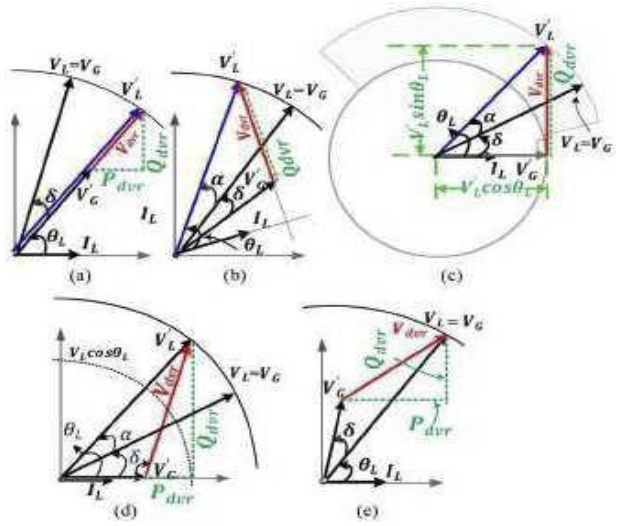

Fig. 2 (a) In-phase injection. (b) Quadrature injection. (c) Quadrature injection limiting case. (d) Energy-optimized injection. (e) Presag injection.

To avoid the problem of over modulation, in the case of deeper sag depth, an iterative loop is employed in the control block. It is found that the proposed method can result in more than 50% additional sag support time when compared with the method in [16] and [17]. The performance of the proposed method is validated using simulation as well as experimental.

II. OVERVIEW OF DVR OPERATION

In this section, different sag compensation approaches [12] - 15] are briefly discussed. The phasor representations of these methods are given in Fig. 2. The phasors VG and VG represent the rated and sagged grid voltages, respectively, whereas VL and VL are the load voltages before and after the sag. To effectively highlight the differences among these methods, PD V R and QD V R are also incorporated in the phasor diagrams. This is mainly to illustrate the amount of active and reactive powers demanded by each method. All of the quantities are drawn considering the load current (I L) as reference phasor.

A. In-Phase Compensation

In this type of compensation, DVR injects the smallest possible voltage magnitude in phase with the sagged grid voltage. However, as seen from Fig. 2(a), this method cannot correct the phase jump. The DVR-injected voltage magnitude and angle are given as

$$V_{DVR} = 2(V_L - V_G) \quad (1)$$

$$\angle V_{DVR} = \theta_L. \quad (2)$$

B. Quadrature Injection (Reactive Compensation)

In this method, the DVR injects voltage in quadrature with the load current, i.e., it corrects the sag with only reactive power. Using Fig. 2(b), the injected voltage magnitude and angle are given as

$$V_{DVR} = 2\ V_L + V_G^2 - 2V_L V_G \cos(\alpha + \delta) \quad (3)$$

$$\angle V_{DVR} = \frac{\pi}{2} \quad (4)$$

where δ is the phase jump in the grid voltage due to the sag and α is the phase jump induced due to reactive power compensation. As reported in [12], the maximum sag depth (Δ Vsag,max) that can be compensated using quartered injection is closely related with the load power factor and can be expressed as

Fig. 2(c) shows the limiting case for quadrature injection where DVR supports the full load reactive power while the grid operates at unity power factor.

C. Energy-Optimized Injection

This method is developed in [15] to enhance the performance of the quadrature injection method for the sag depth deeper than the limit in (5), where the DVR injects certain active power. The DVR voltage magnitude and injection angle can be calculated from Fig. 2(d)

$$\Delta V_{sag-max} \le (1 - \cos\theta_L). \quad (5)$$

D. Presag Compensation

In this method, both load voltage magnitude and phase are restored to presag values. Unlike the previous methods in Fig. 2(a), (b), and (d), the presag method in Fig. 2(e) can successfully compensate the phase jump. However, this phase jump correction requires an additional active power from the dc link capacitor.

$$V_{DVR-max} = V_G \quad (6)$$

$$V_{DVR} = 2\ V_L^2 + V_G^2 - 2V_L V_G \cos(\theta_L) \quad (7)$$

A positive phase jump leads to an increase in angle between the grid voltage and the load current, increasing the active power burden on DVR compared to negative phase jump.

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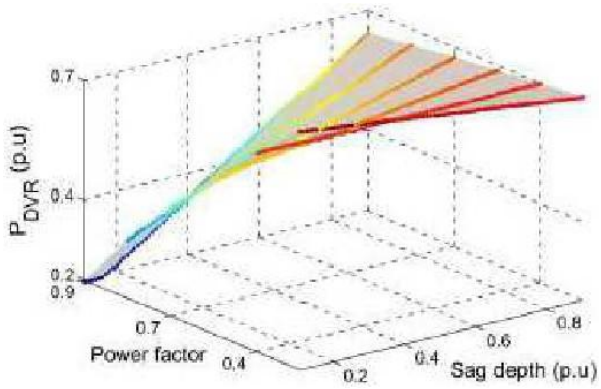

Fig. 3 Active power associated with the presag compensation method for different sag depths (phase jump = 25^0).

III. POWER FLOW ANALYSIS AND MAXIMUM COMPENSATION TIME

As explained earlier, the presag method is the most energy-intensive method, and the injected power can be quite high even for shallow sag depths. Based on the phasor diagram of Fig. 2(e) [(9) and (10)], the active power associated with the presag method can be expressed in terms of sag depth, phase jump, and load power factor as given in the following:

Ppresag = 3VLL (cos(θL)−(1 − Δ Vsag) cos(θL − δ) Fig. 3 shows the DVR active power for a range of variation in sag depth (0.1 ≤ Δ Vsag ≤ 0.9) and power factor (0.4 ≤ cos θL ≤0.9). The phase jump δ is fixed at +25°. As seen from the graph of Fig. 3, the active power supplied by DVR is relatively high (> 0.4 p.u.) for the presag method. The theoretical power flow analysis conducted previously holds true as long as there is a significant amount of energy in the dc link capacitor. However, in the actual system, since it has a finite amount of energy, the voltage across the dc link capacitor Vdc reduces. The following relationship should be satisfied at all time in order to achieve the adequate operation of DVR-VSI [18]:

Vdvr is the injected phase to neutral voltage. Vdc is the dc link voltage. As soon as the dc link voltage decreases below Vdc−min, i.e., the limit set by the DVR controller must stop the compensation process to avoid harmonics contamination in the load voltage.

Considering a lossless DVR system, the dc power in can be equated with the ac power to find the capacitor size. However, owing to the flow of active power, the dc link voltage drops, and the limit can be violated. This limitation restrains the DVR operation even though there is sufficient amount of stored energy in the dc link capacitor as shown in Fig.4. Furthermore, the gradient of the dc link voltage dvdc/dt is directly proportional to the DVR-injected active power, i.e., Pdvr. The lower the value of Pdvr, the smaller is the slope of the dc link voltage and the higher will be the time for which Vdvr/nt ≤ (mi−maxVdc)/2. This leads to the following two hypotheses.

1) The energy stored in the dc link capacitor can further be utilized.
2) The rate of change (fall) of the dc link voltage can further be optimized. This brings another important variable in the power flow analysis which is the "maximum compensation time tc−max." It is the direct measure of "useful" stored charge/energy in the dc link capacitor.

IV. PROPOSED COMPENSATION SCHEME

The work presented in this paper proposes an enhanced sag compensation method to extend the DVR compensation time. It optimizes the gradient of the dc link voltage (dvdc/dt) by regulating the amount of active power injected by DVR. In the proposed method, the controller restores both phase and amplitude of the load voltage to the presag value and then initiates a transition toward the minimum active power (MAP) mode. The overall operation sequence and implementation of the proposed compensation method is discussed in the following subsections.

A. Phase Jump Detection and Presag Restoration

For detecting the phase jump, two PLLs are employed (one over the load voltage and another over the source voltage), giving θV L and θV g, respectively. As soon as the sag is detected, the first step is to determine the DVR initial injection angle that avoids the phase jump at the load side. This is done by freezing the load voltage PLL that gives the presag angle (θV Lp). On the other hand, the unrestricted grid voltage PLL gives the grid voltage phase (θV g). The difference between these two angles gives the initial angle of injection. But in the steady state, both angles will be identical, and thus, the difference will be zero.For sag detection, the absolute difference between the reference load voltage (1 p.u.) and the actual grid voltage (p.u.) in synchronous reference frame is calculated [7], [19]–[22].

B. Controlled Transition toward the MAP Mode

Once the presag voltage is successfully restored, after one cycle, a smooth transition toward the MAP mode is initiated and completed over the next one to two cycles. The self-supporting mode of operation in which the DVR absorbs active power (relatively very small amount) from the grid to overcome the system losses and thus maintains a constant voltage across the dc link capacitor. The term γ indicates the reduction in θ due to loss component and is determined by the dc link (PI) controller. The second part represents a case where the self-supported dc link cannot be maintained due the constraint in (5). To ensure a smooth changeover, a transition ramp is defined between the initial and final operating points, as given in the following:

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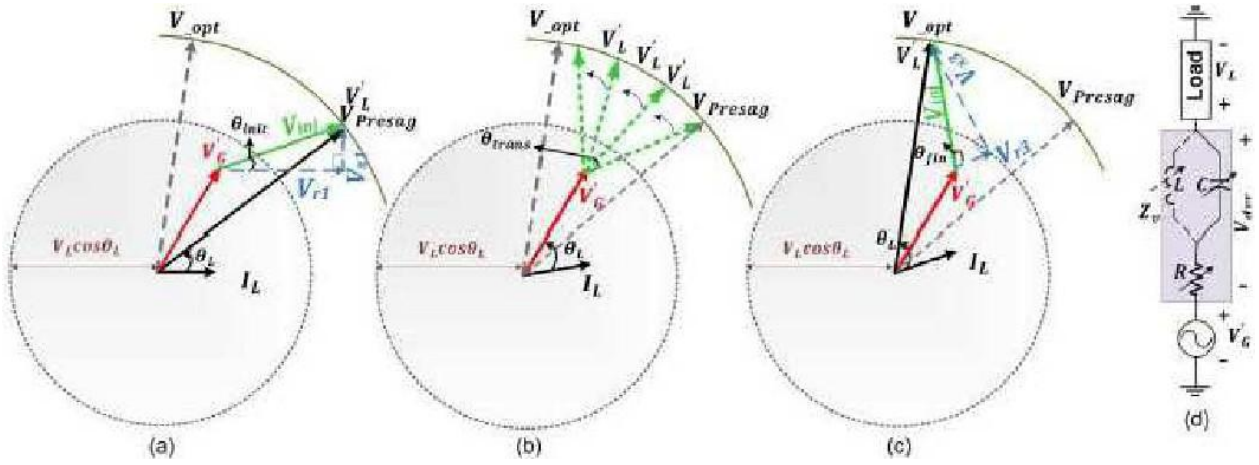

Fig. 5. Phasor diagram for the proposed sag compensation method. (a) Presag restoration, (b) intermediate transition, (c) final load voltage with MAP injection, and (d) DVR visualization as the variable virtual impedance changes from resistive to dominant capacitive (for sag) or inductive (for swell).

$$\theta \xrightarrow{T} \Delta^{(t)}\theta_{\text{init}}$$

C. Iterative Decrement in Injection Angle

In self-supporting mode, the DVR can compensate the sag for an indefinitely long time. However, for deeper sag depths, there is certain nonzero active power injected by DVR. This causes a reduction in the energy stored in the dc link capacitor, and consequently, its voltage reduces (gradually). To maintain the required voltage at the inverter output side, the controller increases the modulation index mi until it reaches mi−max. This is the limiting case as explained by (12), beyond which the controller goes into over modulation and cannot maintain the rated load voltage. To avoid this over modulation condition, an iterative control loop is used, which constantly monitors the dc link voltage and decreases θ in (18) to keep Vdc > Vdc−min.

D. Operation Sequence

TABLE I DVR SYSTEM PARAMETERS (BOUNDARY CONDITIONS)

Parameter	Value
Grid voltage (L-L) (rms) V_{base}	415 V
Line frequency	50 Hz
Nominal Power (Base kVA)	10 kVA
Nominal Load power factor	0.7 Lagging
Maximum compensation time	10 cycles
Maximum sag depth	0.5 p.u
Maximum phase jump	$\pm 45^0$
Maximum injected voltage	0.7 p.u
Transformer turns ratio	1:1
DC link Capacitance value	9000 μF

Fig. 5(a)–(c) depicts the overall operation sequence of the proposed phase jump compensation scheme. The transitionfrom high active power mode (presag) to MAP mode is shown in three steps. The illustration is for the case where the sag depth is more than the limit in (5) and there is a positive phase jump associated with the sag. As discussed previously and shown in Fig. 5(a), DVR initiates the compensation by supplying high active power to the load and restores both magnitude and phase of the load voltage to presag values. After one cycle, the transition toward the MAP mode is initiated, and DVR gradually increases the contribution of reactive power. As seen from Fig. 5(b) and (c), the injected voltage magnitude and its phase angle are gradually increasing until VL reaches VL − opt.

V. ANALYTICAL STUDY ON COMPENSATION TIME WITH DIFFERENT APPROACHES

In this section, a comparative study is presented to determine the maximum compensation time achieved using the aforementioned phase jump compensation methods.

These include the following: 1) the presag; 2) the method given in [16], named as presag–in-phase in this paper; and 3) the proposed method. Table I shows the various design parameters used for the comparison. The maximum compensation time of 200 ms (10 cycles) with a phase jump of +45◦ is taken as reference. Using (15), the value of the dc link capacitor is obtained as 9000 μF.

The sag depth is varied over a range of values from 10% to 80% of nominal grid voltage, keeping the power factor and phase jump fixed at 0.7 lagging and +45◦, respectively. Analytically computed DVR-injected magnitude and maximum compensation times are provided in Fig. 6. Note that the DVR voltage magnitudes are shown after the first one cycle of compensation as all of the three methods perform identically for the first cycle. As seen from Fig. 6(b), both the presage and proposed

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methods have the same VDVR magnitude for a sag depth greater than the limit in (6), i.e., 30%. However, as noticed from Fig. 6(a), tc−max is highest for the proposed method for all values of sag depths. For the designed range of 50% sag depth, it can be seen that the presag–in-phase method improves the compensation time from 10 to 16 cycles over the presag method.

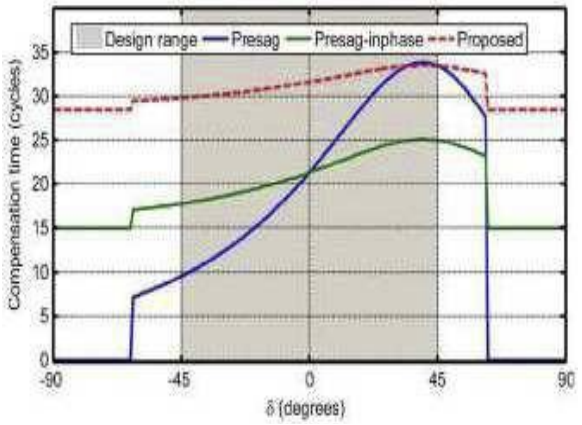

Fig. 6. Maximum compensation time and DVR-injected voltage for various sag depths with different methods. (a) Compensation time cycles. (b) V D V R p.u.

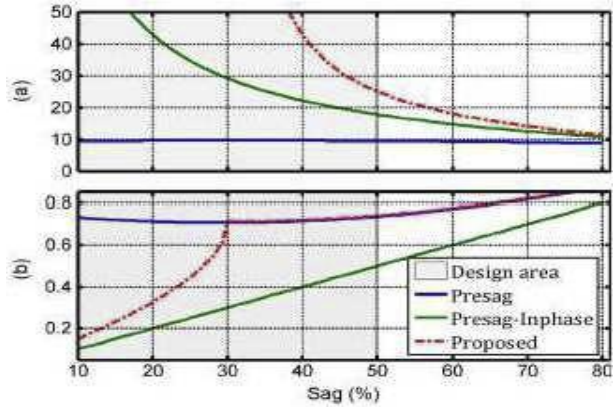

Fig. 7. Maximum compensation time for a range of variation in phase jump

The proposed method further improves it to 22 cycles. Moreover, for the sag depth lower than 30%, the proposed method can withstand any sag duration by operating in the self-supporting mode. The significant improvement in the compensation time is due to the least possible utilization of dc link active power, thus resulting in the slowest discharging of the dc link capacitor. Note that the proposed method does not result in higher injection voltage magnitude than the design limit of 0.7 p.u., which is clear in Fig. 6(b). Fig. 7 depicts the scenario where the phase jump is varied from -90^0 to $+90^0$ for a sag depth of 0.5 p.u. and other boundary conditions from Table I. As seen from the graph, the maximum compensation time is highest for the proposed method. It can also be noted that the presag method becomes unable to correct the phase jump beyond -60^0 and $+6^0$ due to violation of (12).

VI. OVERALL DVR SYSTEM CONTROL SCHEME

Fig. 8 depicts the detailed block diagram of the proposed phase jump compensation method. A logic unit is employed to constantly monitor the grid voltage for sag detection using. To obtain the reference load voltage, the control system is divided into two sub-modules: 1) phase jump detection plus DVR injection angle calculation and (2) MAP injection. To achieve a decoupled active and reactive power control, the phase of the line current is considered as the reference and is obtained by the PLL. The phase jump detection block computes the DVR initial (presag injection) angle and final (MAP injection) angle. Once the transition is over, the MAP block gives the reference voltage VL−abc = Vopt. As shown in Fig. 8, the obtained DVR reference voltage Vdvr is compared with the actual voltage in the stationary reference frame. A proportional-resonant (PR) controller with a large gain at the grid fundamental frequency is used for accurate tracking of Vdvr. To compensate for DVR system losses, Vdvr is added as a feed forward signal to the output of the PR controller. The dc link voltage is constantly monitored in an iterative control loop to regulate the injected voltage angle, thus avoiding over modulation. Note that this block is only required when the sag depth is close to the system design limit.

VII. EVALUATION

The effectiveness of the proposed method is evaluated through MATLAB/Simulink-based simulation study and, lastly, validated on a scaled laboratory prototype experimentally.

A. Simulation Study

A simulation model for the DVR system, with the parameter given in Table I, is developed and simulated for the performance evaluation. The dc link capacitor of 9000 μF, as computed in the previous section, is used for this study. As the intention is to maintain the rated voltage across the load terminals without any phase jump, the sensitive load is represented by an R−L load. The simulation results for two different scenarios are given in Figs. 9 and 10. In the first scenario, a sag depth of 50% [higher than the limit in (5)] is considered with a phase jump of $+25^0$. Asymmetrical voltage sag, for ten cycles, is initiated at time t = 0.1 s [Fig. 9(a)]. As noticed from Fig. 9(b), the load does not see any change in the voltage phase or magnitude. The DVR injected voltage and active–reactive power profiles are shown in Fig. 9(c) and (d), respectively. It can be noticed that the DVR restores the phase jump by injecting the maximum active power at the beginning, and the controller gradually shifts to the MAP mode after one cycle. Fig. 9(e) shows a constant drop in dc link voltage; however, once the controller goes into MAP mode, a slower fall rate can be noticed In the second scenario, a sag depth of 23% [lower than the limit given in (5)] is considered with a phase jump of $+25^0$. As seen from

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the results in Fig. 10, the DVR successfully compensates the load voltage phase and magnitude with the proposed method. Since the voltage sag depth is lower than the limit in (5), the controller settles in the self-supporting mode. A reduction in dc link voltage can be seen [Fig. 10(e)] during the first two cycles (phase jump restoration plus transition period), but as the controller moves into self-supporting mode, the dc link voltage is regulated back to the reference value.

This can be noticed from Fig. 10(d) as well, where the injected active power is positive for the first two cycles and negative onward (self-supporting mode). Furthermore, the study was extended to compute the maximum achievable compensation time, for the existing system, with the proposed method. It is found that the compensation time can be extended from 10 to 25 cycles for the worst case scenario.

Further enhancement in compensation time (more than 25 cycles) will be achieved for intermediate sag depths. Additionally, based on the designed criteria of ten cycles for the new installation, the proposed method can reduce the dc link capacitor size from 9000 to 4200 µF (details given in Appendix C).

B. Experimental Validation

A scaled experimental prototype is developed using digital signal processor (DSP) DS1103 dSPACE and Semikron AN 8005 VSI. The experimental system data are given in Table II. The DSP sampling time of 40 µs is used to run the algorithm in real time. Using the programmable voltage source, a sag depth of 35% with $+25^0$ jump in the voltage phase is initiated. The experimental results for different sag compensation schemes are given in Figs. 11–13.

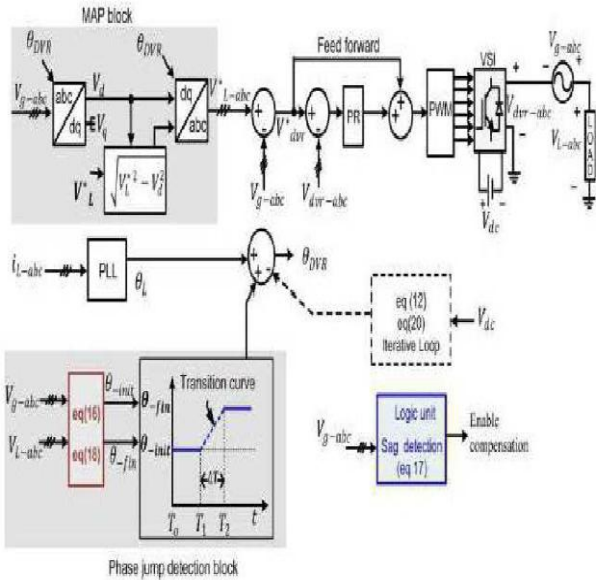

Fig.8.Detailed block diagram of the proposed phase jump compensation method with MAP injection

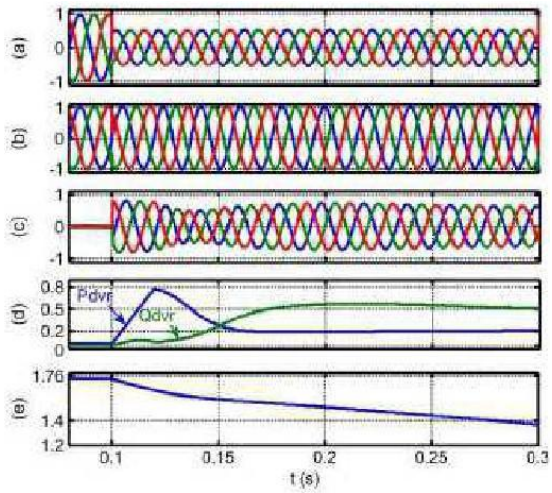

Fig 9. Simulation results for the proposed sag compensation method for 50% sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage, (d) DVR active and reactive power. (e) DC link voltage.

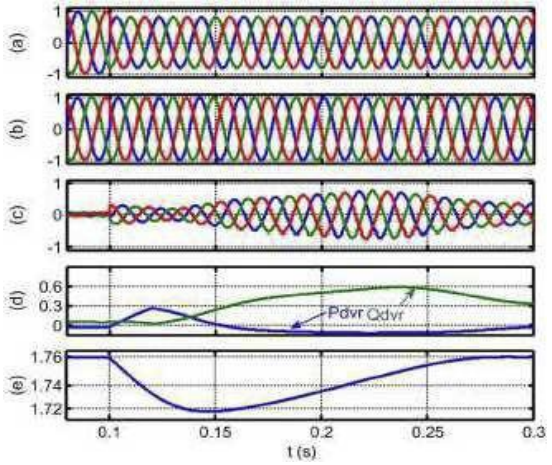

Fig. 10. Simulation results for the proposed sag compensation method for 23% sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage. (d) DVR active and reactive power. (e) DC link voltage.

TABLE II DVR SYSTEM DATA FOR THE EXPERIMENTAL STUDY

Source Chroma 61703	Supply voltage: 50 V-rms, 50 Hz Source Impedance: R_g = 0.047 Ω and L_g = 160 µH
DVR	DC link capacitors, C_{dc} = 1100 µF Reference DC link voltage = 55 V Filter inductor, L_f = 5 mH C_f =50 µF Transformer turns ratio 1:1
Load	R = 11 Ω and L = 80 mH Nominal Load voltage = 50 V Rating = 250 W
Compensation time	10 cycles (200 ms)

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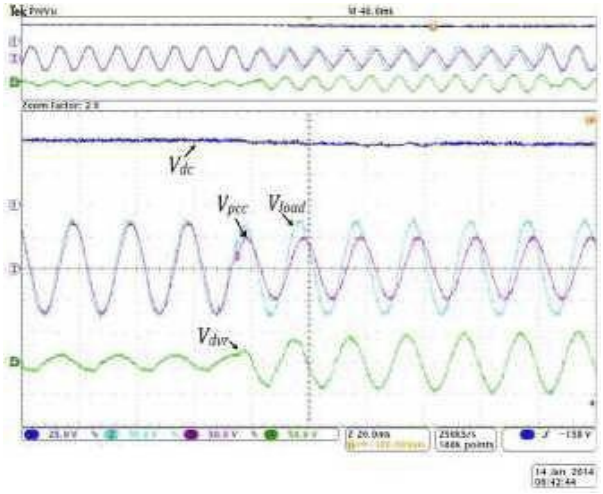

Fig 11 Experimental results for 35% sag depth with +25◦ phase jump using the presag compensation method.

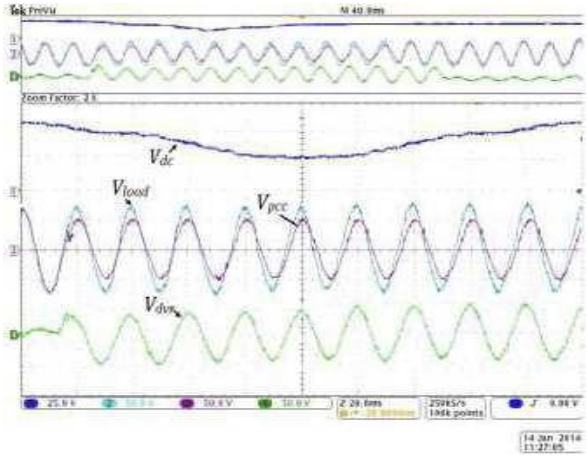

Fig. 12. Experimental results for 35% sag depth with +25◦ phase jump using the quadrature injection method

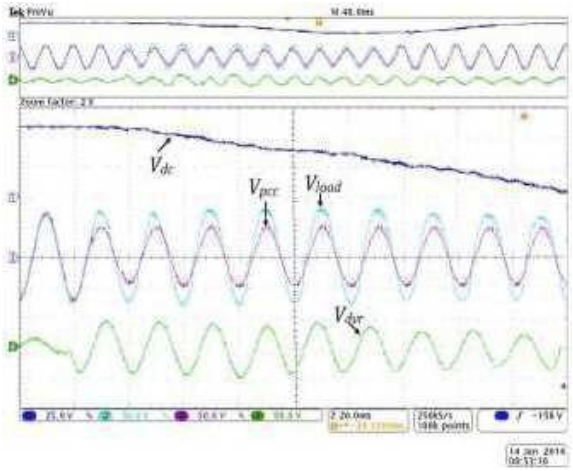

Fig. 13. Experimental results for 35% sag depth with +25◦ phase jump using the proposed method.

Fig. 11 shows the performance of the presag method. It can be seen that the load voltage does not see any transient in the magnitude as well as phase. However, due to the active power injection, there is rapid reduction in the dc link voltage. After seven cycles (lower cycles due to the losses associated with the DVR system), the dc link voltage is dropped to less than 15 V, which consequently decreases the injected voltage magnitude, and as a result, DVR fails to maintain the rated load voltage. For the same sag condition, the performance of the quadrature injection method is given in Fig. 12. The phase jump goes uncompensated; however, it compensates the sag, effectively maintaining the load voltage at rated value while regulating the dc link voltage. Finally, Fig. 13 demonstrates the performance of the proposed method.

As viewed from Fig. 13, the DVR begins compensation by restoring the load voltage and phase to the presag values. There is reduction in dc link voltage due to the requirement of active power for phase jump compensation. Note that the first stage is temporary and lasts for two cycles (after compensation begins). After the first two cycles (from Fig. 13), the proposed controller initiates the transition towards MAP (in this case, toward self- supporting mode since $\Delta V_{sag} \leq (1 - \cos \theta_L)$). This transition (discussed in Fig. 5) can be confirmed by observing the relative phase angle difference between the source and load voltage waveforms. The corresponding increase in the injected voltage magnitude and slow fall rate of the dc link voltage can also be observed. This intermediate transition stage lasts for another two and half cycles. Finally, the proposed controller proceeds to operate in the self-supporting mode to gradually restore the dc link voltage back to the reference value. The corresponding increase in the injected voltage magnitude to recover the dc link voltage can also be noticed from Fig. 13.The aforementioned experimental investigation effectively demonstrates the applicability and feasibility of the proposed phase jump compensation method that can extend the compensation duration of DVR.

VIII. CONCLUSION

In this paper, an enhanced sag compensation scheme has been proposed for the capacitor-supported DVR. The proposed strategy improves the voltage quality of sensitive loads by protecting them against the grid voltage sags involving the phase jump. It also increases compensation time by operating in MAP mode through a controlled transition once the phase jump is compensated. To illustrate the effectiveness of the proposed method, an analytical comparison has been carried out with the existing phase jump compensation schemes. It is shown that the compensation time can be extended from 10 to 25 cycles (considering presag injection as the reference method) for the designed limit of 50% sag depth with 45° phase jump. Further extension in compensation time can be achieved for intermediate sag depths. This extended compensation time can be seen as a considerable reduction in dc link capacitor size (for the studied case more than 50%) for the new installation. The effectiveness of the proposed method has been evaluated through extensive simulations in MATLAB/Simulink and validated on a scaled laboratory

prototype experimentally. The experimental results demonstrate the feasibility of the proposed phase jump compensation method for practical applications.

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